REMARKS/ARGUMENTS

This paper is submitted in response to the non-final Office Action dated February 2, 2007. At that time, claims 1, 2, 4-12, 14-23, and 25-31 were pending in the application. In the Office Action, the Examiner rejected claims 1, 2, 4-12, 14-23 and 25-31 under 35 U.S.C. § 103(a) as being unpatenable over U.S. Patent No. 6,499,054 issued to Hesslink (hereinafter "Hesslink") in view of U.S. Patent No. 6,028,412 in view of Shine (hereinafter "Shine").

By this paper, Applicants respectfully respond to the issues raised by the Office Action. Favorable consideration is respectfully requested.

I. Interview

Applicants would like to thank the Examiner for conducting an in-person interview regarding this case on March 21, 2007. Present for this interview were the Examiner Jennenifer L. Norton, Applicants' attorney Craig J. Madson, and one of the inventors, Walter E. Red ("Dr. Red"). During the interview, a proposed amended claim set was shown to the Examiner. This proposed claim set was discussed by the parties at length. This claim set is being submitted formally herewith via the present paper. Applicants also argued that Hesslink and Shine do not teach the claim element of "executing control software in the host device to generate control input parameters for the controlled device." No agreement was reached during the interview. The Examiner did indicate that she would reserve judgment on Applicants' amendments and arguments until Applicants filed such amendments/arguments formally in a written response. Accordingly, Applicants are submitting these amendments/arguments formally via the present paper. Favorable consideration is respectfully requested.

In the interview, Dr. Red provided the Examiner with a comparison chart of the differences between the present application and Hesslink and Shine. For convenience, a copy of this paper is submitted herewith as Exhibit 1. Dr. Red showed a poster which further shows the differences between the present application and Hesslink and Shine. For convenience, a color copy of this poster is attached hereto as Exhibit 2. Further, Dr. Red also identified a prior art reference to the Examiner regarding a control frequency that is assigned a value of 2^N. A copy of

this reference has been submitted via a Supplemental Information Disclosure Statement and is also attached hereto as Exhibit 3.

II. Rejection Based Upon Hesslink and Shine

The Examiner rejected all of the pending claims under 35 U.S.C. § 103(a) based on Hesslink and Shine. This rejection is respectfully traversed.

The M.P.E.P. states that

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.
>
> The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

M.P.E.P. § 2142.

Applicants respectfully submit that the claims at issue are patentably distinct from the cited references. The cited references do not teach or suggest all of the elements in these claims. Independent claims 1, 11, and 22 all have been amended to recite the step of "executing control software in the host device to generate control input parameters for the controlled device." Support for this claim element is found throughout Applicants' specification, including at Figures 2 and 3, paragraphs [0036][1] through [0038], paragraph [0033], and paragraphs [0047] through [0048].

Such a claim element is not taught or suggested by Hesslink or Shine. Specifically, the Examiner has not indicated, nor can the Applicants find, any supposed teaching in Shine

[1] These paragraph numbers are given with respect to Applicants' published specification, which is found as U.S. Patent Publication No. 2005/0226192.

regarding executing control software in the host device to generate control input parameters for the controlled device. With respect to Hesslink, this reference also fails to teach or suggest this claim language. Specifically, this claim element clearly requires that "control software" be present "in the host device" [computer] that is executed. When executed, this control software generates control input parameters for the controlled device. As explained by the specification, this control software on the host device means that the controlled device does not need to contain any type of controller or hardware interface in order to operate. Rather, the controlled device will be controlled by the software executed on the host computer.

On the other hand, Hesslink teaches using a computer through which a user may control a laser. *See* Hesslink, Col. 3, line 38. However, there is no teaching in Hesslink of any type of "control software," let alone control software being executed on the host device in the manner recited in the claims. In fact, to the extent that Hesslink's laser 64 is being controlled by "control software," any and all such software is being executed by the "interface 62 or interface 74." This interface 62 (or interface 74) is hardware that will control the laser 64. This interface 62 (or interface 74) is hardware that is clearly not on the host computer (and is located remote from the host device).

Thus, it is clear that neither Hesslink nor Shine teach "executing control software in the host device to generate control input parameters for the controlled device" as required by independent claims 1, 11, and 22. Accordingly, Applicants respectfully submit that independent claims 1, 11, and 22 are patentably distinct from the cited references. Withdrawal of this rejection is respectfully requested.

Claims 2 and 4-10 depend either directly or indirectly from independent claim 1. Claims 12 and 14-21 depend either directly or indirectly from independent claim 11. Claims 23 and 25-31 depend either directly or indirectly from independent claim 22. Accordingly, Applicants respectfully request that the rejection of dependent claims 2, 4-10, 12, 14-21, 23, and 25-31 be withdrawn for at least the same reasons as those presented above in connection with claims 1, 11, and 22.

Independent claims 1, 11, and 22 have been amended to provide clarity and to more particularly point out and claim the present subject matter. Further, the claim language regarding the 2^N time slicing algorithm has been removed from the independent claims and has been

moved to dependent claims 4, 14, and 25. Similarly, the other dependent claims that refer to this 2^N time slicing algorithm have been amended to depend from claim 4, claim 14, or claim 25. Favorable consideration is respectfully requested.

III. Conclusion

Applicants respectfully requests that a timely Notice of Allowance be issued in this case. If there are any remaining issues preventing allowance of the pending claims that may be clarified by telephone, the Examiner is requested to call the undersigned.

Respectfully submitted,

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Date: 12 April 2007

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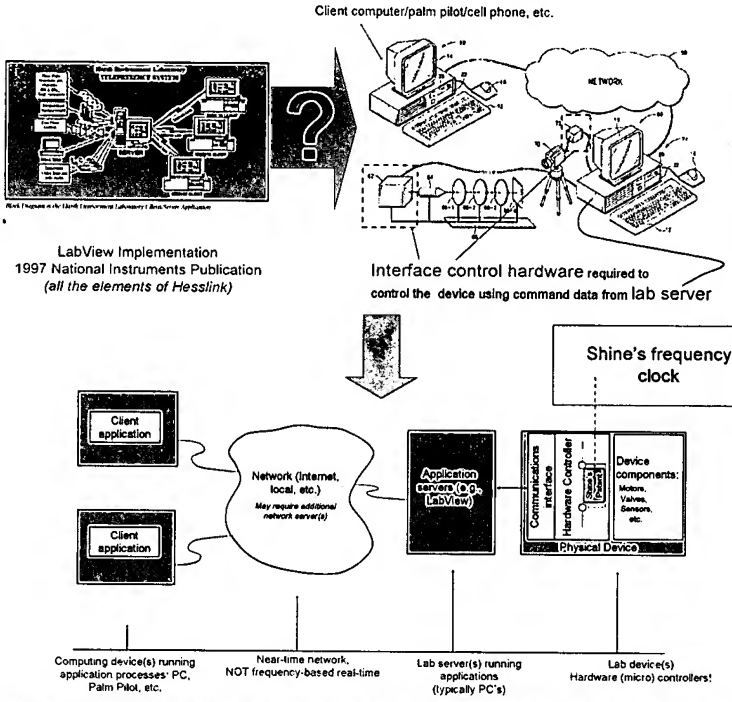
VMAC Comparison to Hesslink/Shine

VMAC Core Features	Red et al.Claims	Hesslink	Shine
Eliminate device hardware (micro) controllers.	Claim 1, 2, 7, etc. (implied, since control loops closed at host control device in software) See BACKGROUND and DETAILED DESCRIPTION.	NO Hesslink teaches the use of existing hardware controllers.	NO Shine teaches a frequency generator to be embedded in an IC or hardware controller using 2^N register comparisons.
Central control host runs software-based real-time control processes at specified frequencies, replacing device hardware controllers.	Claim 1, 4, 5, 6, 11 etc. Real-time is implicit since capable of running 2^N frequencies*. Also described in DETAILED DESCRIPTION.	NO Hesslink teaches several host devices (computers) including client process hosts, and servers. Hesslink does not teach a central host running frequency-based real-time processes, controlling device components over a network, eliminating device micro-controllers.	NO Shine does not teach a central control host running one or more software-based device control processes at specified device frequencies, replacing device hardware controllers.
Central control host closes servo-control loops over real-time network to device components.	Claim 1, 3, 13, 18 Also described in DETAILED DESCRIPTION.	NO Hesslink does not teach servo-control over networks to device components; rather teaches conventional network monitoring of and commands to hardware device controllers through lab servers.	NO Shine does not teach distributed network communications or control; rather teaches a frequency based clock system that is integrated into control hardware for controlling a device.
Devices can be controlled at different frequencies over network from central control host.	Claim 1, 4, 5, 6, etc. Also described in DETAILED DESCRIPTION.	NO Hesslink does not teach control of devices at specified frequencies, rather teaches control through existing device hardware.	NO Shine teaches generating a control frequency required for a device through an IC or microcontroller. He does not teach a central host controlling one or more devices at different frequencies concurrently.

* NOTE: *2^N as a frequency generator is not a critical VMAC claim element, since there are other methods for generating unique frequencies, e.g., 2N*

Hesslink Patent



Shine Patent

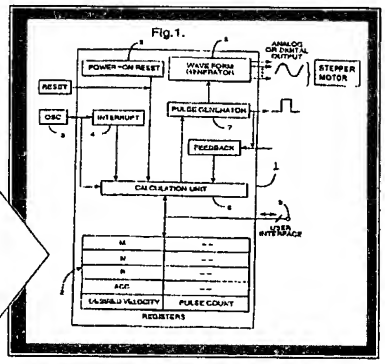
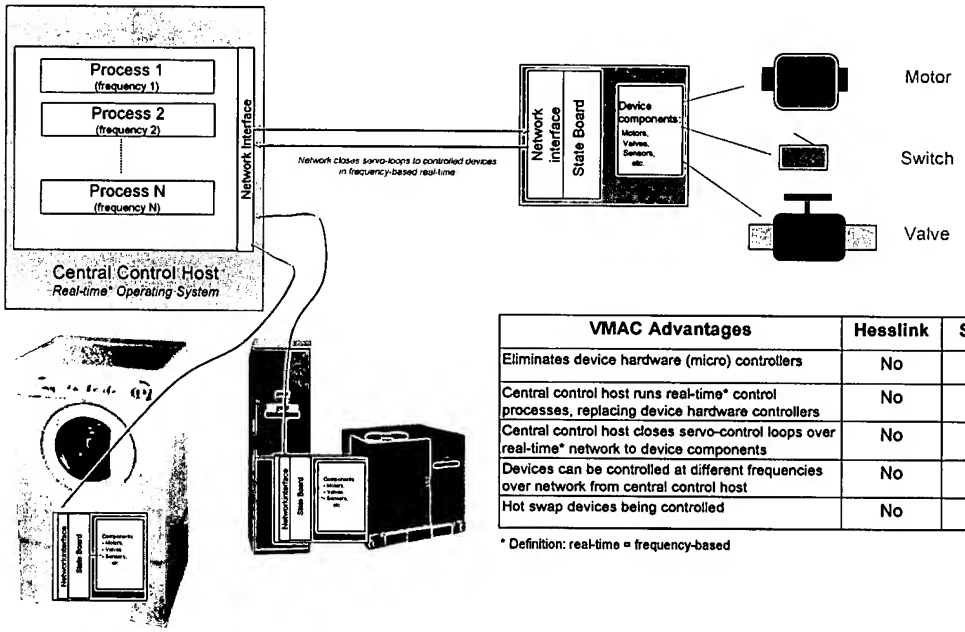


FIG. 1 shows a micro-controller embodying the present invention;

Shine developed a method to generate a required frequency for device control using 2^N register comparisons. The method is to be embedded into a control board/IC.

NOTE: ***Red et al developed the VMAC methods to eliminate control hardware!***

SIMPLICITY OF VMAC CONTROL



VMAC Advantages	Hesslink	Shine
Eliminates device hardware (micro) controllers	No	No
Central control host runs real-time* control processes, replacing device hardware controllers	No	No
Central control host closes servo-control loops over real-time* network to device components	No	No
Devices can be controlled at different frequencies over network from central control host	No	No
Hot swap devices being controlled	No	No

* Definition: real-time = frequency-based

MICROCOMPUTERS AND MODERN CONTROL ENGINEERING

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set. This will also need an *instruction register* in which the instruction fetched from memory can be held while it is being decoded.

Figure 7-5 is a picture of the things we have developed so far and how they might be connected to one another.

Steered by the instruction decoder, numbers may be fetched from the memory and placed in the program counter (to cause the program to branch), in the memory address register (to be used as the addresses of any location in the memory), or in the accumulator or any of the "general-purpose" registers (B, C, etc.) we might include in our complement of hardware. Numbers may also be transferred from registers to the ALU, for arithmetic and logical operations, and back again.

Because it is devoted to processing numbers, logical terms, and instructions (and to distinguish it from the memory and other items of equipment we may add), we will call everything in Fig. 7-5 except the memory the *central processing unit* and abbreviate it "CPU."

The names we chose for the parts of this computer are the names commonly used for them by engineers and programmers. It is evident that many variations and refinements of this arrangement are possible—additional registers might be useful, more powerful instructions might be added, different ways of interfacing between the memory and the CPU might yield a higher performance design, and so on. We see some examples of these in the next chapter, where we examine the designs of several actual microcomputers.

SIZE

Computers are often referred to as "8-bit," "16-bit," and "32-bit" computers. There are also "4-bit," "12-bit," and "24-bit" computers. When used in this way, these terms refer to the number of bits in the principal general-purpose registers and accumulator of the CPU. The most commonly used computers have register sizes that are multiples of eight bits. These are not necessarily representative of the majority of the world population of computers, because most of the microcomputers used in the ubiquitous pocket calculators are of the 4-bit type. Some computers have mixed register sizes.

The optimum size of a register depends on how it is to be used and, most particularly, on the number of *states* needed—that is, the number of numbers that it must be able to represent. A register of n bits has 2^n possible states. The table below lists several common sizes and their number of possible states:

n	*States*	n	*States*
4	16	16	65536
8	256	24	16777216
12	4096	32	4294967296

Clearly, the more bits in a register, the more resolution and dynamic range it has. A 32-bit computer can perform computations to more than nine significant digits. It can count up to the estimated world population as of 1978.

In talking about these numbers, the symbol "K" is used to stand for $2^{10} = 1024$ (very close to the number 1000, for which "k" is sometimes used). Thus, a 16-bit register has

$$2^{16} = 2^6 \cdot 2^{10} = 64 \cdot 1024 = 64\text{K} \qquad (7.13)$$

possible states. This is a popular size for program counters and memory address registers in many computers, allowing them to specify 65536 distinct memory locations.

The optimum size of a register is a compromise between hardware cost and the degree to which high resolution and wide dynamic range are actually needed. If the computer is to be applied to complex computational problems in which high resolution and wide dynamic range are important (e.g., weather prediction, astrophysics, quantum physics), it will be most convenient for its programmers if it is equipped with "wide" registers. If the computer is to be applied to a simple control problem in which resolution to only about 0.5 percent is needed, then 8-bit registers will generally suffice and will cost less.

If, from time to time, a program must handle numbers that will not "fit" within one of its registers, the programmer can use *multiple-precision* techniques: treating a pair or triplet of registers as if they were concatenated, with an implied factor of the appropriate power of 2 applied to the most significant of the pair. Although there may be added costs for these approaches, they are generally less than the cost of making *every* register in the computer wide enough to handle every number it might encounter.

Most numbers handled by most programs are less than 256. This range allows us to represent the letters of the English alphabet (and also many non-English alphabets), numerals, punctuation marks, and so on, using the ASCII code or similar codes. It allows us to count or total many commonly used quantities (e.g., the number of steps in one revolution of a stepping motor, the degree to which a valve is open to within about 0.5 percent). Thus, 8-bit registers are a reasonable compromise found in many computers.

These 8-bit numbers are called *bytes*. (In an even lighter vein, 4-bit numbers are then called "*nibbles*" by some, although this term has not attained the same official stature in the jargon as has the term "byte.")

Because 8-bit numbers are so common, it has become widespread practice to organize memories around this size. The use of "byte-

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 12, 2007.

Attorney for Applicant(s)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/823,465	Confirmation No.: 4603
Applicant	:	Walter E. Red et al.	
Title	:	SYSTEMS AND METHODS FOR CONTROLLING AND MONITORING MULTIPLE ELECTRONIC DEVICES	
Filed	:	April 13, 2004	
TC/A.U.	:	2121	
Examiner	:	Jennifer L. Norton	
Docket No.	:	1737.2.15	
Customer No.	:	21552	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Transmitted herewith is an Information Disclosure Statement disclosing information which has come to the attention of applicants and/or their attorneys and is being submitted so as to comply with the duty of disclosure set forth in 37 C.F.R. § 1.56. In accordance with 37 C.F.R. § 1.97(c), the enclosed Statement is being filed before the mailing date of either a final action or a notice of allowance and is accompanied by credit card payment form in the amount of One Hundred Eighty Dollars ($180.00) to cover the fee set forth in 37 C.F.R. § 1.17(p).

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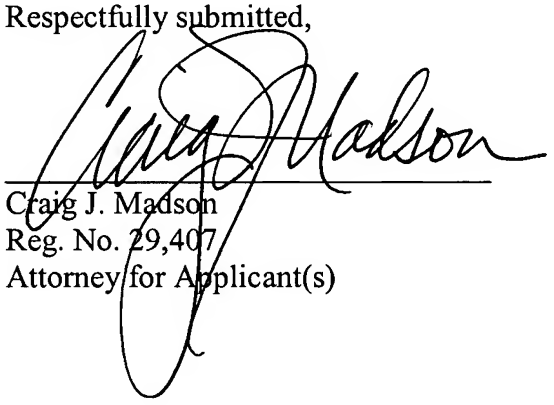
Neither applicants nor their attorneys make any representation that any information disclosed herein may be "prior art" within the meaning of that term under 35 U.S.C. § 102 or § 103. Moreover, pursuant to 37 C.F.R. § 1.97, the filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made or as an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b).

In accordance with 37 C.F.R. § 1.98, transmitted herewith are:

1. A completed copy of Form(s) PTO/SB/08a and/or PTO/SB08b "Information Disclosure Statement by Applicant" listing the patents, publications and other information being submitted for consideration; and

2. A legible copy of each patent, publication and other item of information in written form listed on the enclosed Form(s) PTO/SB/08a and PTO/SB/08b, except for copies of U.S. patents and published U.S. patent applications which are not required for applications filed after June 30, 2003.

Respectfully submitted,



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